Electronic Version
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Claims

[c1] 1. A method for fabricating a non-volatile memory, the method comprising:
providing a substrate;
forming a mask layer over the substrate;
forming a trench in the mask layer and the substrate;
forming a tunnel dielectric layer in the trench;
forming a floating gate in the trench;
removing the mask layer;
forming a high-voltage doped region in the substrate on one side of the floating gate, the high-voltage doped region serving as a first source/drain region and a control gate; and
forming a second source/drain region in the substrate on another side of the floating gate.

[c2] 2. The method of claim 1, further comprising:
forming a gate dielectric layer over the substrate; and
forming a select gate on said the other side of the floating gate, the select gate being located between the second source/drain region and the floating gate and being isolated from the substrate by the gate dielectric layer.

[c3] 3. The method of claim 2, wherein the floating gate is a

doped silicon layer, and the method further comprising:
performing a thermal oxidation process to form a thermal oxide layer on top of the floating gate after the floating gate is formed, wherein the thermal oxide layer has a shape such that the floating gate has sharp edges; and
forming spacers on exposed sidewalls of the floating gate after the mask layer is removed.

[c4] 4. The method of claim 3, wherein the spacers comprise oxide/nitride/oxide (ONO) composite spacers.

[c5] 5. The method of claim 1, wherein a bottom of the high-voltage doped region is as deep as a bottom of the floating gate.

[c6] 6. The method of claim 1, wherein the high-voltage doped region extends to a region underneath the floating gate.

[c7] 7. The method of claim 1, wherein the floating gate completely fills the trench.

[c8] 8. A method for fabricating a non-volatile memory, the method comprising the steps of:
providing a substrate;
forming a mask layer over the substrate;
forming a pair of trenches in the mask layer and the

substrate;

forming a tunnel dielectric layer in each trench;

forming a floating gate in each trench;

removing the mask layer;

forming spacers on exposed sidewalls of each floating gate;

forming a high-voltage doped region in the substrate between the trenches, the high-voltage doped region serving as a common source/drain region and a control gate;

forming a gate dielectric layer over the substrate;

forming a select gate on an outward-facing side of each floating gate, the select gate being isolated from the substrate by the gate dielectric layer; and

forming a source/drain region in the substrate on an outward-facing side of each select gate.

[c9] 9. The method of claim 8, wherein each floating gate is a doped silicon layer, and the method further comprising:

performing a thermal oxidation process to form a thermal oxide layer on top of each floating gate after the floating gates are formed, wherein the thermal oxide layer has a shape such that the floating gate has sharp edges, wherein

the select gates at least cover a portion of the floating gates, and upper portions of the select gates are isolated

from the top of the floating gates by the thermal oxide layers and lower portions of the select gates are isolated from the sidewalls of the floating gates by the spacers.

[c10] 10. The method of claim 8, wherein each spacer comprises an oxide/nitride/oxide (ONO) composite spacer.

[c11] 11. The method of claim 8, wherein a bottom of the high-voltage doped region is as deep as bottoms of the floating gates.

[c12] 12. The method of claim 8, wherein the high-voltage doped region extends to a region underneath each floating gate.

[c13] 13. The method of claim 8, wherein each floating gate completely fills the corresponding trench.

[c14] 14. A non-volatile memory, comprising:
a substrate with a trench therein;
a tunnel dielectric layer in the trench;
a floating gate that completely fills the trench and protrudes beyond the substrate;
a high-voltage doped region in the substrate on one side of the floating gate, serving as a first source/drain region and a control gate; and
a second source/drain region in the substrate on an other side of the floating gate.

[c15] 15. The non-volatile memory of claim 14, wherein the memory further comprises:
a gate dielectric layer over the substrate;
a select gate located on said other side of the floating gate between the floating gate and the second source/drain region, being isolated from the substrate by the gate dielectric layer.

[c16] 16. The non-volatile memory of claim 15, wherein
the floating gate is a doped silicon layer with an oxide layer on its top portion and spacers on its sidewalls, wherein the oxide layer has a shape such that the floating gate has sharp edges, and
the select gate at least covers a portion of the floating gate, and an upper portion of the select gate is isolated from the top of the floating gate by the oxide layer and a lower portion of the select gate is isolated from the sidewall of the floating gate by the spacer.

[c17] 17. The non-volatile memory of claim 16, wherein the spacers comprise oxide/nitride/oxide (ONO) composite spacers.

[c18] 18. The non-volatile memory of claim 14, wherein a bottom of the high-voltage doped region is as deep as a bottom of the floating gate.

[c19] 19. The non-volatile memory of claim 14, wherein the high-voltage doped region extends to a region underneath the floating gate.

[c20] 20. A non-volatile memory, comprising:
a substrate with a pair of trenches therein;
a tunnel dielectric layer in each trench;
a pair of floating gates each filling a trench and protruding beyond the substrate, wherein sidewalls of each floating gate is disposed with spacers;
a high-voltage doped region in the substrate between the floating gates, serving as a common source/drain region and a control gate;
a pair of select gates on outward-facing sides of the floating gates, wherein each select gate is isolated from the substrate by a gate dielectric layer; and
a pair of source/drain regions in the substrate on outward-facing sides of the select gates.

[c21] 21. The non-volatile memory of claim 20, wherein each floating gate is a doped polysilicon layer with a thermal oxidation layer on itstop portion, wherein the thermal oxide layer has a shape such that each floating gate has sharp edges, and
the select gates at least covers a portion of the floating gates, and upper portions of the select gates are isolated

from the top of the floating gates by the thermal oxidation layers and lower portions of the select gates are isolated from the sidewalls of the floating gates by the spacers.

[c22] 22. The non-volatile memory of claim 20, wherein each spacer comprises an oxide/nitride/oxide (ONO) composite spacer.

[c23] 23. The non-volatile memory of claim 20, wherein a bottom the high-voltage doped region is as deep as bottoms of the floating gates.

[c24] 24. The non-volatile memory of claim 20, wherein the high-voltage doped region extends to a region underneath each floating gate.